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MICROCOMPUTER MN103S

# MN103S65G

# LSI Application Note Excerption

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# About This Manual

## ■Composition of this book

This LSI application note explains in order of the sample program which used the program collection which uses the circumference circuit of MN103S65G loading, and 3-phase PWM.

## ■Composition as a manual

This book is roughly divided and consists of a title, the text, a sample program, an inclusion directory, cautions information, and reference information.

Next, the layout and definition of each portion are shown.

1.Inside title

2.Small title

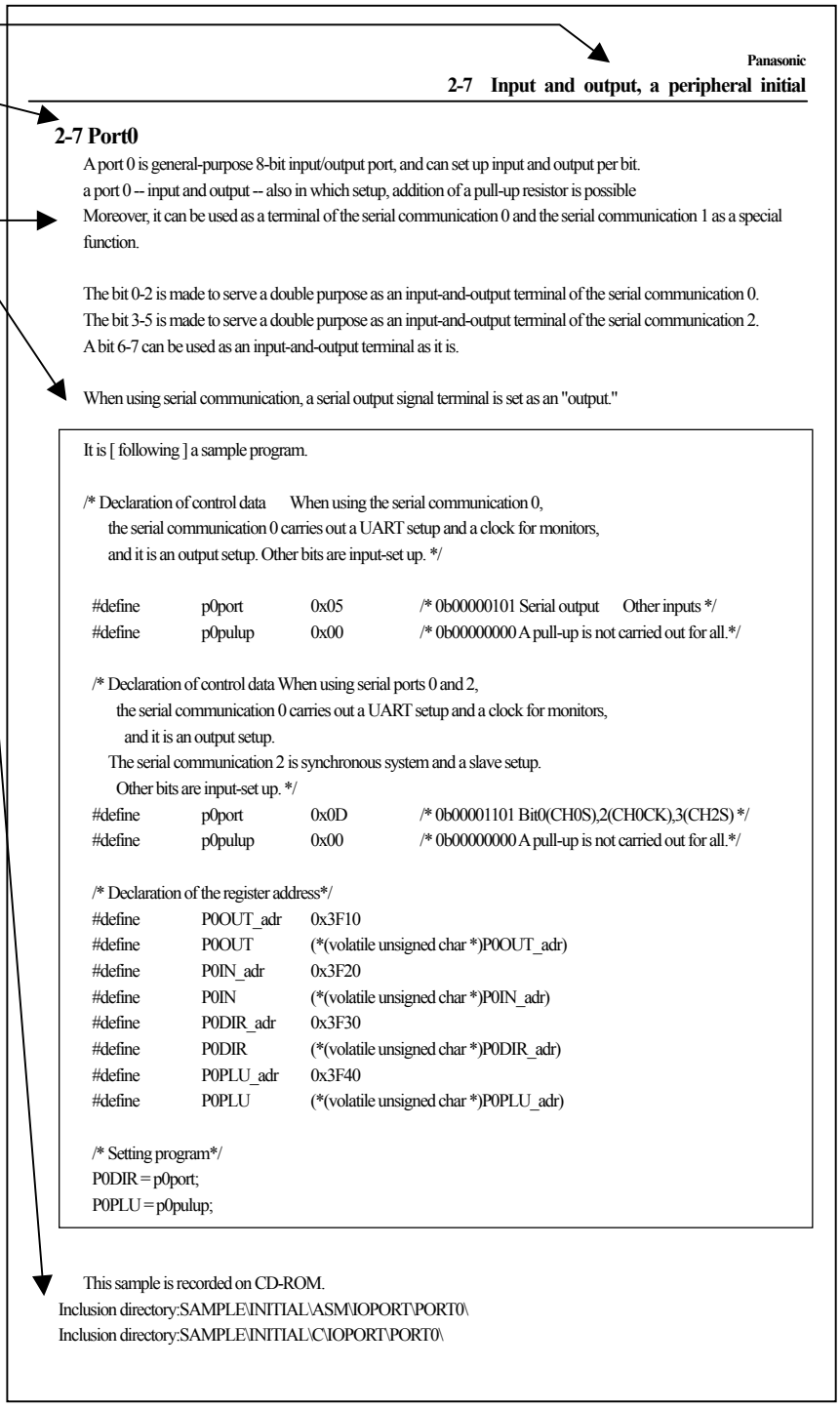
It is the minimum block of this book.

3.Text

4.Sample program

5.Inclusion directory

The inclusion directory is shown although the sample program is recorded on CD-ROM.



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**2-7 Input and output, a peripheral initial**

**2-7 Port0**

A port 0 is general-purpose 8-bit input/output port, and can set up input and output per bit.
a port 0 -- input and output -- also in which setup, addition of a pull-up resistor is possible
Moreover, it can be used as a terminal of the serial communication 0 and the serial communication 1 as a special function.

The bit 0-2 is made to serve a double purpose as an input-and-output terminal of the serial communication 0.
The bit 3-5 is made to serve a double purpose as an input-and-output terminal of the serial communication 2.
A bit 6-7 can be used as an input-and-output terminal as it is.

When using serial communication, a serial output signal terminal is set as an "output."

It is [ following ] a sample program.

```
/* Declaration of control data      When using the serial communication 0,
    the serial communication 0 carries out a UART setup and a clock for monitors,
    and it is an output setup. Other bits are input-set up. */

 #define        p0port          0x05            /* 0b00000101 Serial output     Other inputs */
 #define        p0pulup         0x00            /* 0b00000000 A pull-up is not carried out for all.*/

 /* Declaration of control data When using serial ports 0 and 2,
     the serial communication 0 carries out a UART setup and a clock for monitors,
      and it is an output setup.
    The serial communication 2 is synchronous system and a slave setup.
     Other bits are input-set up. */
 #define        p0port          0x0D            /* 0b00001101 Bit0(CH0S),2(CH0CK),3(CH2S) */
 #define        p0pulup         0x00            /* 0b00000000 A pull-up is not carried out for all.*/

 /* Declaration of the register address*/
 #define        P0OUT_adr       0x3F10
 #define        P0OUT           (*(volatile unsigned char *)P0OUT_adr)
 #define        P0IN_adr        0x3F20
 #define        P0IN            (*(volatile unsigned char *)P0IN_adr)
 #define        P0DIR_adr       0x3F30
 #define        P0DIR           (*(volatile unsigned char *)P0DIR_adr)
 #define        P0PLU_adr       0x3F40
 #define        P0PLU           (*(volatile unsigned char *)P0PLU_adr)

 /* Setting program*/
 P0DIR = p0port;
 P0PLU = p0pulup;
```

This sample is recorded on CD-ROM.
Inclusion directory:SAMPLE\INITIAL\ASM\IOPORT\PORT0\
Inclusion directory:SAMPLE\INITIAL\C\IOPORT\PORT0\

The example of this page is a thing for explanation. It differs from an actual page.

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## Chapter1 Initialization of the memory at the time of a power supply injection (power-on boot)

## Chapter2 Each peripheral initial by C

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# 2-4 A 8-bit 16-bit timer, a peripheral initial

## 2-4-1 The various registers of a 8-bit timer

Book LSI contains eight 8-bit timers, and is an interval timer, an event timer counter, and a clock output. It can be used as the standard clock of a serial interface, and start timing of A/D conversion.

These timers can perform cascade connection use of a maximum of four.

### ●Timer register

It is the 8-bit register which counts a timer. A count value can be read by the down counter.

TM0BC,TM1BC,TM3BC,TM4BC,TM5BC,TM6BC,TM7BC

### ●Timer mode register

It is the 8-bit register which sets up the mode of a timer of operation.
The clock source which can be chosen by each timer is different. Be careful of a setup.

TM0D: Timer 0 mode register
Bit7 : Count operation permission
0: A stop of operation
1: Permission of operation

Bit6 : Base register setup
0: Usually, operation
1: Initialization
The value of a base register is loaded to a binary counter.
The timer pulse output 0 is reset on a low level.

Bit5-3: Prohibition (0 fixation)

Bit2-0: Clock source selection
000:IOCLK
001:IOCLK/8
010:IOCLK/32
011: Prohibition of a setup
100: Prohibition of a setup
101: Timer 1 underflow

110: Timer 1 underflow
111: TMIN0 terminal input

TM1MD: Timer 1 mode register
Bit7 : Count operation permission
0: A stop of operation
1: Permission of operation

Bit6 : Base register setup
0: Usually, operation
1: Initialization
The value of a base register is loaded to a binary counter.

The timer pulse output 1 is reset on a low level.

Prohibition (0 fixation)

Bit 2-0: Clock source selection
000:IOCLK
001:IOCLK/8
010:IOCLK/32
011: Cascade connection with a timer 0
100: Timer 0 underflow
101: Prohibition of a setup
110: Timer 2 underflow
111: TMIN1 terminal input

TM2MD: Timer 2 mode register
Bit7 : Timer operation permission
0: A stop of operation
1: Permission of operation

Bit6 : Timer initialization
0: Usually, operation
1: Initialization
The value of a base register is loaded to a binary counter.
The timer pulse output 2 is reset on a low level.

Bit 5-3: Prohibition (0 fixation)

Bit2-0: Clock source selection
000:IOCLK
001:IOCLK/8
010:IOCLK/32
011: Cascade connection with a timer 1
100: Timer 0 underflow

101: Timer 1 underflow
110: Prohibition of a setup
111: TMIN2 terminal input

TM3MD: Timer 3 mode register
Bit7 : Timer operation permission
0: Stop of operation
1: Initialization

Bit6 : Timer initialization
0: Usually, operation
1: Initialization
The value of a base register is loaded to a binary counter.
The timer pulse output 3 is reset on a low level.

Bit5-3: Prohibition (0 fixation)

Bit2-0: Clock source selection
000:IOCLK
001:IOCLK/8
010:IOCLK/32
011: Cascade connection with a timer 2
100: Timer 0 underflow
101: Timer 1 underflow
110: Timer 0 underflow
111: TMIN3 terminal input

TM4MD: Timer 4 mode register
Bit7 : Timer operation permission
0: Stop of operation
1: Permission of operation

Bit6 : Timer initialization
0: Usually, operation
1: Initialization
The value of a base register is loaded to a binary counter.
The timer pulse output 4 is reset on a low level.

Bit5-3: Prohibition (0 fixation)

Bit2-0: Clock source selection
000:IOCLK
001:IOCLK/8
010:IOCLK/32
011: Prohibition of a setup
100: Prohibition of a setup
101: Timer 5 underflow

110: Timer 6 underflow
111: TMIN4 terminal input

TM5MD: Timer 5 mode register
Bit7 : Timer operation permission
0: Stop of operation
1: Permission of operation

Bit6 : Timer initialization
0: Usually, operation
1: Initialization
The value of a base register is loaded to a binary counter.
The timer pulse output 5 is reset on a low level.
Bit5-3: Prohibition (0 fixation)

Bit2-0: Clock source selection
000:IOCLK
001:IOCLK/8
010:IOCLK/32
011: Cascade connection with a timer 4
100: Timer 4 underflow
101: Prohibition of a setup
110: Timer 6 underflow
111: TM5IN terminal input

TM6MD: Timer 6 mode register
Bit7 : Timer operation permission
0: Stop of operation
1: Permission of operation

Bit6 : Timer initialization
0: Usually, operation
1: Initialization
The value of a base register is loaded to a binary counter.
The timer pulse output 6 is reset on a low level.

Bit5-3: Prohibition (0 fixation)

Bit2-0: Clock source selection
000:IOCLK
001:IOCLK/8
010:IOCLK/32
011: Cascade connection with a timer 5
100: Timer 4 underflow
101: Timer 5 underflow
110: Prohibition of a setup

111: TM6IN terminal input

TM7MD: Timer 7 mode register

Bit7 : Timer operation permission

0: Stop of operation

1: Permission of operation

Bit6 : Timer initialization

0: Usually, operation

1: Initialization

The value of a base register is loaded to a binary counter.

The timer pulse output 7 is reset on a low level.

Bit5-3: Prohibition (0 fixation)

Bit2-0: Clock source selection

000:IOCLK

001:IOCLK/8

010:IOCLK/32

011: Cascade connection with a timer 6

100: Timer 4 underflow

101: Timer 5 underflow

110: Timer 6 underflow

111: TM7IN terminal input

TMMPSC: Prescaler mode register

Bit7 : Count operation permission

0: Stop of operation

1: Permission of operation

To use 1/8SYSCLK, and 1/32SYSCLK, a Prescaler control register needs to be set up.

When a TMnIO terminal input is chosen, the rising edge of a terminal input is counted.

TMEXPSC8: External Prescaler control register

Bit03-01: Count source selection (timers 0, 2, and 4)

0:TMINn terminal input

1:IOCLK/128

Bit00 : Prescaler (1 / 128 operation permission)

0: Stop of operation

1: Permission of operation

●Various setup of a 8-bit timer

It is a setup when using it as an interval timer.

```
/*******************************
* Register address
*******************************/

/* Timer 0 register address declaration */
#define TM0BC           (*((volatile unsigned char *)0x0000A150))
#define TM0BR           (*((volatile unsigned char *)0x0000A148))
#define TM0MD           (*((volatile unsigned char *)0x0000A140))

/* Timer 1 register address declaration */
#define TM1BC           (*((volatile unsigned char *)0x0000A151))
#define TM1BR           (*((volatile unsigned char *)0x0000A149))
#define TM1MD           (*((volatile unsigned char *)0x0000A141))

/* Timer 2 register address declaration */
#define TM2BC           (*((volatile unsigned char *)0x0000A154))
#define TM2BR           (*((volatile unsigned char *)0x0000A14C))
#define TM2MD           (*((volatile unsigned char *)0x0000A144))

/* Timer 3 register address declaration */
#define TM3BC           (*((volatile unsigned char *)0x0000A155))
#define TM3BR           (*((volatile unsigned char *)0x0000A14D))
#define TM3MD           (*((volatile unsigned char *)0x0000A145))

/* Timer 4 register address declaration */
#define TM4BC           (*((volatile unsigned char *)0x0000A170))
#define TM4BR           (*((volatile unsigned char *)0x0000A168))
#define TM4MD           (*((volatile unsigned char *)0x0000A160))

/* Timer 5 register address declaration */
#define TM5BC           (*((volatile unsigned char *)0x0000A171))
#define TM5BR           (*((volatile unsigned char *)0x0000A169))
#define TM5MD           (*((volatile unsigned char *)0x0000A161))

/* Timer 6 register address declaration */
#define TM6BC           (*((volatile unsigned char *)0x0000A174))
#define TM6BR           (*((volatile unsigned char *)0x0000A16C))
#define TM6MD           (*((volatile unsigned char *)0x0000A164))

/* Timer 7 register address declaration */
#define TM7BC           (*((volatile unsigned char *)0x0000A175))
#define TM7BR           (*((volatile unsigned char *)0x0000A16D))
#define TM7MD           (*((volatile unsigned char *)0x0000A165))

/* Pre-scaler register address declaration */
/* timer 0-3 */
#define TM03PSC         (*((volatile unsigned char *)0x0000A158))
/* timer 4-7 */
#define TM47PSC         (*((volatile unsigned char *)0x0000A178))
/* pre-scaler control register*/
#define TMEXPSC8        (*((volatile unsigned char *)0x0000A17C))

/* Declaration of setting data */
#define TM0MD_STOP      0x00        /* timer stop */
```

```
#define TM0_COUNT4        3            /* cycles/min ratio setup (4 cycles/min -1)    */
#define TM0MD_LOAD1       0x07         /* TMIN0 Terminal input setup */

#define TM0MD_STABLE1 0x00         /* stabilization */
#define TM0MD_START1    0x40         /* timer start */
#define TM0MD_ENABLE1 0x80         /* timer permission*/

#define PS0MD_STOP        0x00       /* pre-scaler stop */
#define PS0MD_START       0x80       /* pre-scaler start*/

#define TM1MD_STOP        0x00       /* timer stop*/
#define TM1_COUNT3        5          /* cycles/min ratio setup (5 cycles/min -1)    */
#define TM1MD_LOAD1       0x03       /* load cycles/min ratio*/
#define TM1MD_STABLE1 0x00       /* stabilization */
#define TM1MD_START1    0x40       /* timer start */
#define TM1MD_ENABLE1 0x80       /* timer permission*/

#define PS0_COUNT200    199        /* cycles/min setup (200 cycles/min-1)    */
#define TM0_COUNT0x5f 0x5f       /* cycles/min setup (0xea5f = 0xea60(60000) - 1) */
#define TM1_COUNT0xea 0xea       /* cycles/min setup (0xea5f = 0xea60(60000) - 1) */
#define TM0MD_LOAD2       0x42       /* read cycles/min ratio */
                                 /* clock source (pre-scaler 0 clock ) setup */
#define TM1MD_LOAD2       0x03       /* timer 0 and cascade connection*/

#define TM0MD_STABLE2 0x02       /* stabilization*/
#define TM1MD_STABLE2 0x01       /* stabilization*/
#define TM0MD_START2    0x82       /* timer start*/
#define TM1MD_START2    0x81       /* timer start */

/*********************************************
* Interval timer by 8-bit timer
* Pre-scaler 0 is used, and the cascade connection of the timers 0
* and 1 is carried out, and it is used as a 16-bit timer.
*********************************************/
void initInterval8( void )
{
      unsigned short data0,data1;

      TM03PSC = PS0MD_STOP;         /* pre-scaler stop*/
      TM0MD = TM0MD_STOP;             /* timer stop*/
      TM1MD = TM1MD_STOP;             /* timer stop*/

      /* Setup of timer cycles/min ratio 60000-1 */
      TM0BR = TM0_COUNT0x5f;        /* cycles/min setup      0xea5f=59999 */

      TM1BR = TM1_COUNT0xea;        /* cycles/min setup*/

      data0 = 0;
      TM0MD = data0;                /* Arbitrary setup */
      data1 = TM1MD_LOAD2;
      TM1MD = data1;                /* timer 0 and cascade setup */

      data0 |= TM0MD_START1;
      TM0MD = data0;                /* Timer 0 initialization LDE=1 */
      data1 |= TM1MD_START1;
      TM1MD = data1;                /* Timer 1 initialization LDE=1 */

      data0 &= ~TM0MD_START1;
      TM0MD = data0;                /* Timer 0 start    LDE=0 */
```

```
    data1 &= ~TM1MD_START1;
    TM1MD = data1;                  /* Timer 1 start    LDE=0 */

    data1 |= TM1MD_ENABLE1;
    TM1MD = data1;                  /* Timer 1 permission    CNE=1 */
    data0 |= TM0MD_ENABLE1;
    TM0MD = data0;                  /* Timer 0 permission    CNE=1 */

    TM03PSC = PS0MD_START;      /* Pre-scaler start */
    TM0MD = TM0MD_START2;         /* Timer start*/
    TM1MD = TM1MD_START2;         /* Timer start */
}
```

The sample of a 8-bit timer is recorded on attached CD-ROM.
Inclusion director:program\initial\timecounter\timer8\
program :timer8int.c

It is a setup when using it as an event timer.

```
/*********************************
* Register address
*********************************/

/* Timer 0 register address declaration */
#define TM0BC           (*((volatile unsigned char *)0x0000A150))
#define TM0BR           (*((volatile unsigned char *)0x0000A148))
#define TM0MD            (*((volatile unsigned char *)0x0000A140))

/* Timer 1 register address declaration */
#define TM1BC           (*((volatile unsigned char *)0x0000A151))
#define TM1BR           (*((volatile unsigned char *)0x0000A149))
#define TM1MD            (*((volatile unsigned char *)0x0000A141))

/* Timer 2 register address declaration */
#define TM2BC           (*((volatile unsigned char *)0x0000A154))
#define TM2BR           (*((volatile unsigned char *)0x0000A14C))

#define TM2MD            (*((volatile unsigned char *)0x0000A144))

/* Timer 3 register address declaration */
#define TM3BC           (*((volatile unsigned char *)0x0000A155))
#define TM3BR           (*((volatile unsigned char *)0x0000A14D))
#define TM3MD            (*((volatile unsigned char *)0x0000A145))

/* Timer 4 register address declaration */
#define TM4BC           (*((volatile unsigned char *)0x0000A170))
#define TM4BR           (*((volatile unsigned char *)0x0000A168))
#define TM4MD            (*((volatile unsigned char *)0x0000A160))

/* Timer 5 register address declaration */
#define TM5BC           (*((volatile unsigned char *)0x0000A171))
#define TM5BR           (*((volatile unsigned char *)0x0000A169))
#define TM5MD            (*((volatile unsigned char *)0x0000A161))

/* Timer 6 register address declaration */
#define TM6BC           (*((volatile unsigned char *)0x0000A174))
#define TM6BR           (*((volatile unsigned char *)0x0000A16C))
#define TM6MD            (*((volatile unsigned char *)0x0000A164))
```

```
/* Timer 7 register address declaration */
#define TM7BC           (*((volatile unsigned char *)0x0000A175))
#define TM7BR           (*((volatile unsigned char *)0x0000A16D))
#define TM7MD           (*((volatile unsigned char *)0x0000A165))

/* Pre-scaler register address declaration */
/* timer 0-3 */
#define TM03PSC         (*((volatile unsigned char *)0x0000A158))
/* timer 4-7 */
#define TM47PSC         (*((volatile unsigned char *)0x0000A178))
/* Pre-scaler control register */
#define TMEXPSC8        (*((volatile unsigned char *)0x0000A17C))

/* Declaration of setting data */
#define TM0MD_STOP      0x00      /* Timer stop*/
#define TM0_COUNT4      3         /* cycles/min ratio setup (4 cycles/min-1)    */
#define TM0MD_LOAD1     0x07      /* TMIN0 Terminal input setup */

#define TM0MD_STABLE1 0x00        /* Stabilization */
#define TM0MD_START1    0x40      /* timer start*/
#define TM0MD_ENABLE1 0x80        /* Timer permission */

#define PS0MD_STOP      0x00      /* Pre-scaler stop*/
#define PS0MD_START     0x80      /* Pre-scaler start*/

#define TM1MD_STOP      0x00      /* timer stop*/
#define TM1_COUNT3      5         /* cycles/min ratio setup(5 cycles/min-1)    */
#define TM1MD_LOAD1     0x03      /* cycles/min ratio reloaded */
#define TM1MD_STABLE1 0x00        /* stabilization*/

#define TM1MD_START1    0x40      /* timer start*/
#define TM1MD_ENABLE1 0x80        /* timer permission */

#define PS0_COUNT200    199       /* cycles/min ratio setup (200 cycles/min-1)    */
#define TM0_COUNT0x5f 0x5f        /* cycles/min ratio setup (0xea5f = 0xea60(60000) - 1) */
#define TM1_COUNT0xea 0xea        /* cycles/min ratio setup (0xea5f = 0xea60(60000) - 1) */
#define TM0MD_LOAD2     0x42      /* cycles/min ratio reloaded */
                                  /* Clock source (Pre-scaler 0 clock) setup*/
#define TM1MD_LOAD2     0x03      /* timer 0 and cascade connection */

#define TM0MD_STABLE2 0x02        /* stabilization */
#define TM1MD_STABLE2 0x01        /* stabilization */
#define TM0MD_START2    0x82      /* timer start */
#define TM1MD_START2    0x81      /* timer start */

/*********************************************
* Event counter by 8-bit timer
* TMIN0 terminal is carried out for 1 / 4 cycles/min using a timer 0,
* and underflow interruption is generated.
*********************************************/
void initEventCounter8( void )
{
    unsigned short data;

    data   = TM0MD_STOP;
    TM0MD = data;                 /* timer stop */

    /* TM0 underflow interruption is permitted. */
```

```
    /* A port 0 is set as TM0IO (input). */

    TM0BR = TM0_COUNT4;          /* cycles/min ratio setup */
    data |= TM0MD_LOAD1;
    TM0MD = data;                /* count source setup     input TMIN0*/

    data |= TM0MD_START1;
    TM0MD = data;                /* initialize timer LDE=1 */

    data &= ~TM0MD_START1;
    TM0MD = data;                /* Timer start LDE=0 */

    data |= TM0MD_ENABLE1;
    TM0MD = data;                /* Timer permission CNE=1 */
}
```

The sample of a 8-bit timer is recorded on attached CD-ROM.
Inclusion directory:program\initial\timecounter\timer8\
program :timer8evt.c

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